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FOCAL-PLANE ON-LINE NONUNIFORMITY CORRECTION USING FLOATING-GATE ADAPTATION

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ABSTRACT

We develop stochastic adaptive algorithms for on-line correction of spatial nonuniformity in random-access addressable imaging systems. The adaptive architecture is implemented in analog VLSI, integrated with the sensors on the focal plane. Random sequences of address locations selected with predetermined statistics are used to adaptively equalize the intensity distribution at a variable spatial scale. Through a logarithm transformation of system variables, adaptive gain correction is achieved through offset correction in the log-domain. This idea is particularly attractive for compact implementation using translinear floating-gate MOS circuits. The technique applies to a variety of solid-state imagers, such as artifical retinas and IR sensor arrays. Experimental results confirm gain correction in a 64×64 pixel adaptive array integrated on a $2.2mm \times 2.25mm$ chip in 1.2 μm CMOS technology.

1. INTRODUCTION

Since the seminal work by Carver Mead on neuromorphic floating-gate adaptation in the silicon retina [1], few groups have addressed the problem of on-line adaptive correction of nonuniformities on the focal plane in solid-state image sensor arrays [2] and neuromorphic vision sensors [3], while most efforts have concentrated on non-adaptive correction using on-chip [4] or off-chip calibrated storage. Gain and offset nonuniformities in the photosensors and active elements on the focal plane contribute "salt-and-pepper" fixed-pattern noise at the received image, which limit the resolution and sensitivity of imaging systems. Flicker noise and other physical sources of fluctuation and mismatch make it a necessity to correct for these effects *on-line*, which is problematic since the image received is itself unknown. Existing "blind" adaptive algorithms for on-line correction are complex and the amount of computation required to implement them is generally excessive. Integration on the focal plane would incur a significant increase in active pixel size and so a decrease in spatial resolution and fill-factor of the imager along with an increase in power consumption.

In this paper we present a class of stochastic adaptive algorithms which integrate general nonuniformity correction with minimal, if not zero, overhead in the number of active components on the focal plane. In particular, we use floating-gate adaptive CMOS technology combined with translinear circuitry to implement a two-transistor adaptive gain element for on-line focal-plane compensation of (photo-)current gain mismatch. The algorithms make effective use of the statistics of image intensity under randomly selected sequences of address locations, and avoid the need for extra circuitry to *explicitly* compute spatial averages and locally difference the result. The resulting *stochastic* algorithms are particularly simple to implement.

2. ADAPTIVE NONUNIFORMITY CORRECTION

Nonuniformity correction can be approached using two strategies: apply a uniform reference image to the static imager and ensure that all pixel outputs are equal [1], or drift natural scenes across the imager where each pixel subtracts its output from its spatially low-pass filtered output to derive an error signal [5]. The former is referred to as *static* nonuniformity correction (SNUC) and the latter as *scene-based* nonuniformity correction (SBNUC). Our imager can accomodate either type of mismatch correction strategy. The SBNUC algorithm has been implemented on the focal plane in CMOS and IR based imagers [2] and has been successful in reducing offset mismatch.

In this paper, we will concentrate on SNUC to reduce current gain mismatch in a photo-transistor based CMOS imager or silicon retina. We will show how by applying a controllable voltage offset on a floating-gate transistor in each pixel, we achieve an adjustable, adaptive pixel current gain. Our system architecture also allows to perform SBNUC through controlling the statistics of random address sequences.

First we setup the problem in terms of established on-line algorithms for offset correction. Then we show how this same algorithm can be extended to gain mismatch reduction through a simple logarithm transformation of system state variables.

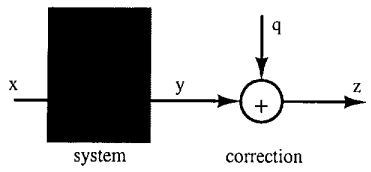

Figure 1: Offset correction

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2.1. Canceling offset nonuniformity

Figure 1 schematically demonstrates the offset correction technique. The set of system equations are:

$$y = x + o, \qquad z = y + q = x + o + q \tag{1}$$

where x is the input random (sensor) variable, y is the received input with unknown offset o, q is the applied offset correction and z is the corrected output. For offset compensation, we want $(o + q) \equiv$ const for all pixels. A simple (gradient descent) adaptive rule to achieve this is [5]:

$$\Delta q = -\alpha\,(z - z_{ref}) \tag{2}$$

which adjusts the output z on average towards a reference constructed by expressing variable degrees of smoothness in the image:

$$z_{ref} = \begin{cases} \langle z \rangle & \text{for SNUC} \\ \langle z \rangle_{local} & \text{for SBNUC} \end{cases} \tag{3}$$

where the $< \cdot >$ symbol represents spatial averaging at global and local scales, respectively, and α denotes the adaptation (or "learning") rate. Circuits implementing a locally differenced diffusive kernel, with adjustable space constant, to perform the computations (2) are presented in [2]. We introduce a stochastic version of the rule in equation (2):

$$\Delta q_{\mathbf{r}(k)} = -\alpha\,\left(z_{\mathbf{r}(k)} - z_{\mathbf{r}(k-1)}\right) \tag{4}$$

where the subscripts $\mathbf{r}(k)$ and $\mathbf{r}(k-1)$ denote pixel addresses at consecutive time steps k and $(k-1)$ respectively. Taking expectations on both sides of equation (4), for a particular pixel selected at time k, yields

$$\mathrm{E}\left[\Delta q_{\mathbf{r}(k)}\right] = -\alpha\left(z_{\mathbf{r}(k)} - \mathrm{E}\left[z_{\mathbf{r}(k-1)}\right]\right)$$

which can be further expanded in terms of the statistics

$$\mathrm{E}\left[z_{\mathbf{r}(k-1)}\right] = \int z_{\mathbf{r}(k-1)} p\left(\mathbf{r}(k-1)|\mathbf{r}(k)\right) d^2\mathbf{r}(k-1)$$

as determined by the conditional transition probabilities (densities) $p\left(\mathbf{r}(k-1)|\mathbf{r}(k)\right)$. Therefore, by controlling the statistics $p\left(\mathbf{r}(k-1)|\mathbf{r}(k)\right)$ through proper choice of the random sequence of addresses $\mathbf{r}$, we can implement, on average, the spatial convolution kernels needed to implement both SNUC and SBNUC in (3). In particular, for a random sequence, $\mathbf{r}(k-1)$ and $\mathbf{r}(k)$ are independent, and

$$\mathrm{E}\left[z_{\mathbf{r}(k-1)}\right] = \langle z \rangle \tag{5}$$

whereas, if $\mathbf{r}(k-1)$ and $\mathbf{r}(k)$ are related by embedding memory in the address sequence (e.g., through inertia, or imposing limits on $\Delta\mathbf{r}$),

$$\mathrm{E}\left[z_{\mathbf{r}(k-1)}\right] = \langle z \rangle_{local}. \tag{6}$$

Equation (4) is a(*stochastic*) on-line version of SNUC and likewise, equation (6) implements stochastic SBNUC. Hardware requirements can be further simplified by thresholding the update (4) into the pilot-rule

$$\Delta q_{\mathbf{r}(k)} = -\alpha\,\mathrm{sign}\left(z_{\mathbf{r}(k)} - z_{\mathbf{r}(k-1)}\right) \tag{7}$$

with fixed-size update increments and decrements.

2.2. Canceling gain nonuniformity

The gradient descent formulation [5] also adaptively compensates for gain mismatch, although it does not prevent the gain from becoming negative. Our approach is to relate gain correction, under the positivity constraint imposed by current-domain circuits, to offset correction through a logarithm transformation. This transformation has a physical meaning which can be exploited in the hardware implementation as discussed in the next section. Figure 2 schematically illustrates the concept of gain mismatch correction in relation to Figure 1.

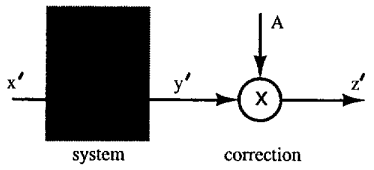

Figure 2: Gain correction

The system is governed by equations:

$$y' = a\,x', \qquad z' = A\,y' = A\,a\,x' \tag{8}$$

which transform into

$$\ln z' = \ln A + \ln a + \ln x', \tag{9}$$

so that for gain nonuniformity correction, $(\ln A + \ln a) \equiv const$ for all pixels. By identifying correspondending terms (in particular, $\ln A = q$ or $A = e^q$ and $\ln a = o$) in equations (1) and (9), and because of the monotonicity of the logarithmic map, the learning rule (7) can be rewritten as:

$$\Delta q_{\mathbf{r}(k)} = -\alpha\,\mathrm{sign}\left(z'_{\mathbf{r}(k)} - z'_{\mathbf{r}(k-1)}\right) \tag{10}$$

which in turn can be expressed as a stochastic on-line learning rule with relative gain increments:

$$\Delta A_{\mathbf{r}(k)} = -\alpha A_{\mathbf{r}(k)}\,\mathrm{sign}\left(z'_{\mathbf{r}(k)} - z'_{\mathbf{r}(k-1)}\right). \tag{11}$$

3. FOCAL-PLANE VLSI IMPLEMENTATION

Rather than implementing (11) directly, we make use of the exponential relationship between voltage and current in a (subthreshold) MOS transistor to encode a current *gain* as the exponential of a differential voltage across a *floating gate* capacitor. The increments and decrements Δq in (10) are then naturally implemented by hot-electron injection and tunneling across the floating gate oxide [6].

3.1. The pixel

The pixel circuit diagram is shown in Figure 3. A vertical *pnp* bipolar transistor converts photon energy to emitter current I_{in} with current gain β. Transistors M_1 and M_2 form a current mirror with adjustable current gain. M_2 is a floating-gate transistor with two control electrodes; V_{in} and V_{EL} are the voltages which, through capacitive coupling, set voltage V_{fg}. V_{EL} is an externally applied global voltage for all pixels. The pixel's output current I_{out} is sourced by transistor M_2 and measured off-chip. Transistor M_3's gate and source provide random access pixel addressing at the periphery, as needed to implement the stochastic kernel.

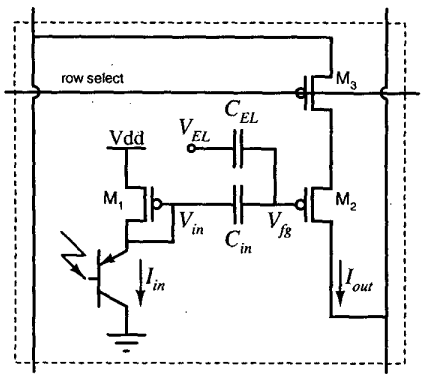

Figure 3: Floating gate adaptive pixel circuit

This design establishes current transfer function in the subthreshold regime:

$$I_{out} = c\ (I_{in})^{1-\lambda} \exp\left(\frac{-\kappa\lambda Q}{C_{EL}V_T}\right) \exp\left(\frac{-\kappa\lambda V_{EL}}{V_T}\right) \quad (12)$$

where $c = (I_0 W/L \exp(V_{dd}/V_T))^{\lambda}$, I_0 is the subthreshold leakage current, W and L are width and length of transistors M_1 and M_2, $\lambda = C_{EL}/(C_{EL} + C_{in}) \approx 0.3$, Q is the charge injected/tunneled onto the floating gate, V_T is the thermal voltage and κ the subthreshold slope factor (back gate coefficient).

The first exponential term on the right in equation (12) corresponds to the adaptive gain correction A, while the second represents a normalization term which is globally controlled by V_{EL}. By injecting electrons onto (tunneling electrons from) the floating gate [6] we incrementally (decrementally) alter Q, which in turn relates logarithmically to A, and thereby effectively implements the pilot rule (10).

3.2. System architecture

Figure 4 illustrates the setup used to experimentally validate the concept of reducing the gain mismatch between pixels on the fabricated prototype adaptive array with 64 × 64 pixels. We uniformly illuminate the imager and randomly select a column and row address $\mathbf{r}(k)$. With switch S_1 closed and S_2 open, we measure $I_{out(\mathbf{r}(k))}$ using a transimpedance amplifier. If $I_{out(\mathbf{r}(k))} < I_{out(\mathbf{r}(k-1))}$, we open S_1 and momentarily close S_2. The drain of transistor M_2 is pulsed down to $V_{inj} \approx (V_{dd} - 8V)$ and a small packet of negative charge is injected onto the floating gate. If $I_{out(\mathbf{r}(k))} \geq I_{out(\mathbf{r}(k-1))}$, we do not alter the gain of the selected pixel and continue by randomly selecting a new pixel. As such we implement a *one-sided* version of the stochastic pilot rule of equation (10):

$$\Delta q_{\mathbf{r}(k)} = \begin{cases} \alpha & I_{out(\mathbf{r}(k))} - I_{out(\mathbf{r}(k-1))} < 0; \\ 0 & \text{otherwise.} \end{cases}$$

Because adaptation is active in only one direction, the average level $\langle I_{out} \rangle$ drifts in that direction over time. We can use the coupling electrode to compensate for this drift.

4. EXPERIMENTAL RESULTS

The 64 × 64 phototransistor-based imager was uniformly illuminated using a white light source. We scanned the pixel array before

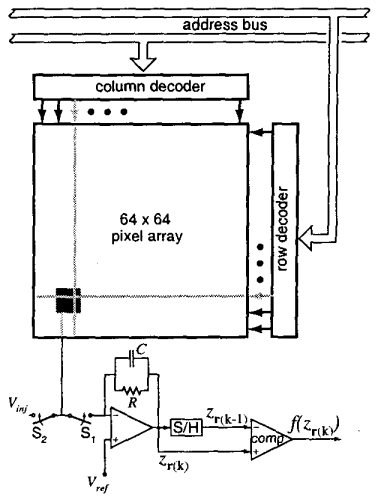

Figure 4: Harware system setup

any gain mismatch correction and again after every 200 cycles of correction until we judged correction to be completed after 2800 cycles. Each of the 4096 pixels were selected every cycle. Figure 5 shows the evolution of histograms of I_{out} versus adaptation cycle number.Also shown are the scanned images before and after gain mismatch correction.

We measured and plotted the standard deviation of I_{out} ($\sigma_{I_{out}}$) divided by the mean I_{out} ($\langle I_{out} \rangle$) versus $\langle I_{out} \rangle$ before and after gain mismatch correction. The five different $\langle I_{out} \rangle$ represent five different levels of illumination 1, 2, 3, 4 and 5. Adaptation was done at illumination level 5. Figure 6 plots these results.

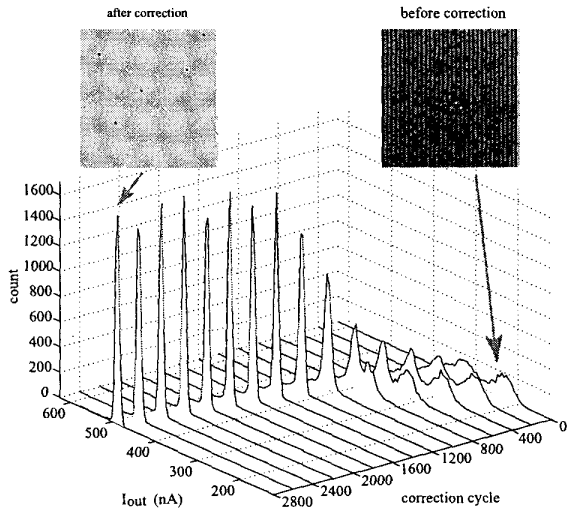

Figure 5: Time course of gain nonuniformity reduction

We projected a black and white $35mm$ slide onto the imager after gain mismatch correction and scanned the array. The slide

contained a light-grey character "R" against a dark-grey background (both bitmapped). We show the resulting scanned image in Figure 7.

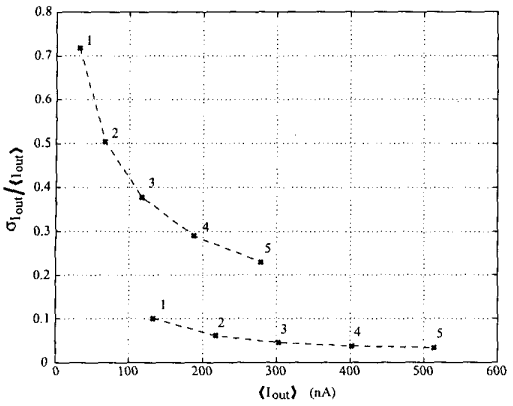

Figure 6: Pre-and-post corrected $\sigma_{I_{out}} / \langle I_{out} \rangle$ versus I_{out} for five different illumination intensities.

5. DISCUSSION

Injecting a negative packet of charge onto the floating gate of transistor M_2 lowers its gate voltage and therefore increases its output current. Consequently, correction is in one direction only, namely increasing the current gain. Since the efficiency of charge injection depends exponentially on the magnitude of drain-source current through the device [6], pixels having higher I_{out} will inject more each time their drains are pulled to V_{inj}. This "positive feedback" effect can be kept in check either by driving the common drain with a current rather than voltage source, or by appropriately setting V_{inj}, keeping S_2 closed for a short time only ($\approx 100\mu sec.$) and having hysteresis in the comparator which compares $I_{out(r(k-1))}$ with $I_{out(r(k))}$. We choose the latter option for simplicity of the test setup, and expect to obtain new results with the former scheme in the near future.

The scanned image before correction in Figure 5 shows strong vertical striations in I_{out}. After the gain mismatch correcton procedure, these striations are no longer visible as evidenced by the post-correction image. We see 5 dark pixels (low I_{out}) in this image. These pixels are "stuck" off and therefore experience negligeable injection when they are selected. Ideally, after correction we should expect to see an impulse in the histogram, all pixels having the same I_{out} when uniformly illuminated. In reality we see a single narrow peak in the histogram due to injection efficiency being proportional to current and due to hysteresis in the comparator.

Figure 6 demonstrates that we did in fact reduce gain mismatch and not just $\sigma_{I_{out}} / \langle I_{out} \rangle$ as a consequence of increasing $\langle I_{out} \rangle$ [7]. The pre-and-post-correction data lie on two separate curves demonstrating that there is indeed a dramatic reduction in gain mismatch due to adaptation. At low $\langle I_{out} \rangle$ (*i.e.* low illumination), there is a reduction in $\sigma_{I_{out}} / \langle I_{out} \rangle$ from 70% to 10%. At higher $\langle I_{out} \rangle$ (*i.e.* high illumination), the reduction is from 24% to 4%.

The scanned image of an "R" after adaptation shown in Figure 7 gives a clear image mostly free of the salt-and-pepper noise usually present in silicon retinas or active pixel sensors.

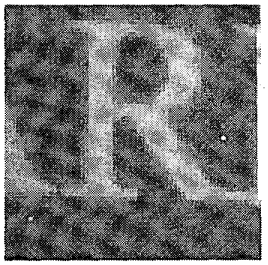

Figure 7: Image after gain mismatch reduction

6. CONCLUSIONS

We have introduced a compact pixel design and a strategy for reducing gain mismatch inherrent in arrays of phototransistors used in CMOS imagers. We have shown how the learning rule for offset correction can be transformed into the log domain to produce a stable learning rule for on-line gain mismatch correction. This rule is very naturally implemented by a simple translinear circuit. The pixel incorporates a floating gate transistor which can be incrementally injected with a small packet of negative charge. The injected charge increases the current gain of the pixel in relative terms (*i.e.*, by constant increments on a logarithmic scale).

Experimental results from a custom 64 × 64 phototransistor-based adaptive pixel CMOS array, fabricated through MOSIS, prove that our pixel design and learning rule were successful for SNUC. We expect to refine and extend the experimental characterization of the prototype chip in the next couple of months, and demonstrate SBNUC for on-line gain mismatch reduction.

7. REFERENCES

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